CLAIMS

What is claimed is:

1. A cross-connect comprising:

a plurality of sets of data input lines, each of said sets of data input lines to be coupled to a different line card; and

a plurality of matrixes each coupled to every of said set of data input lines and each having a set of data output lines, the set of data input lines of each of said plurality of matrices to be coupled to a different one of said line cards.

2. The cross-connect of claim 1, wherein:

the data input lines of each of said sets of data input lines have an order according to a bit position; and

for each of said plurality of matrices,

a plurality of sets of control lines, each matrix entry in a row of the matrix coupled to the same one of said sets of control lines and each matrix entry in a column of the matrix coupled to the same bit position data input line of each of said different line cards to selectively store in any given row of the matrix the data on one of said sets of data input lines; and

the matrix entries of a column are coupled in series to selectively move the data on a row-by-row basis.

3. The cross-connect of claim 2, wherein for each of said plurality of matrices, each matrix entry of a column of said matrix comprises:

a store mux having data inputs coupled to the data input lines coupled to said matrix entry;

a storage element coupled to an output of said store mux to selectively store data on said output of said store mux; and

a shift element coupled to an output of said storage element and an output of the shift element of the preceding matrix entry in the column to selectively move data from shift element to shift element and/or from storage element to shift element in the column.

4. The cross-connect of claim 2, wherein:

for each of said plurality of matrices, said last matrix entry of each of the columns of the matrix collectively provide said set of data outputs of said matrix.

5. A network element comprising:

a plurality of line cards; and

a cross-connect including a plurality of sets of data input lines, each of said sets of data input lines coupled to a different one of said plurality line cards; and

a plurality of matrixes each coupled to every of said set of data input lines and each having a set of data output lines, the set of data input lines of each

of said plurality of matrices to be coupled to a different one of said plurality of line cards.

6. The network element of claim 5, wherein:

the data input lines of each of said sets of data input lines have an order according to a bit position; and

for each of said plurality of matrices,

a plurality of sets of control lines, each matrix entry in a row of the matrix coupled to the same one of said sets of control lines and each matrix entry in a column of the matrix coupled to the same bit position data input line of each of said different line cards to selectively store in any given row of the matrix the data on one of said sets of data input lines; and

the matrix entries of a column are coupled in series to selectively move the data on a row-by-row basis.

7. The network element of claim 6, wherein for each of said plurality of matrices, each matrix entry of a column of said matrix comprises:

a store mux having data inputs coupled to the data input lines coupled to said matrix entry;

a storage element coupled to an output of said store mux to selectively store data on said output of said store mux; and

a shift element coupled to an output of said storage element and an output of the shift element of the preceding matrix entry in the column to selectively

move data from shift element to shift element and/or from storage element to shift element in the column.

8. The network element of claim 6, wherein:

for each of said plurality of matrices, said last matrix entry of each of the columns of the matrix collectively provide said set of data outputs of said matrix.

9. A cross-connect comprising:

a plurality of sets of data input lines, each of said sets of data input lines to be coupled to a different line card, the data input lines of each of said sets of data input lines having an order according to a bit position; and

a plurality of matrixes, for each of said plurality of matrices,

a plurality of sets of control lines, each matrix entry in a row of the matrix coupled to the same one of said sets of control lines, wherein each row is coupled to a different one of said sets of control lines, each matrix entry including,

a space mux, each space mux in a column of the matrix coupled to the same bit position data input line of each of said different line cards,

a storage element coupled to the output of said space mux, and

a shift element coupled to the output of said storage element and the output of the shift element of the preceding matrix entry in the same column.

10. The cross-connect of claim 9, wherein said storage element of a first of said matrix entries comprises:

a store register having an input and an output, said output of said store register coupled to said shift element of said first matrix entry; and

a timing mux having a data input coupled to the output of said space mux, a data input coupled to the output of said store register, a control input coupled to said set of control lines, and an output coupled to the input of said store register.

11. The cross-connect of claim 10, wherein said shift element of said first of said matrix entries comprises:

a shift register having an input and an output, said output of said shift register providing said output of said shift element; and

a shift mux having a data input coupled to the output of the store register of said first matrix entry, a data input coupled to the output of the shift element of the preceding matrix entry in the same column, a control input coupled to said set of control lines, and an output coupled to the input of said shift register.

12. The cross-connect of claim 9, wherein said shift element of a first of said matrix entries comprises:

a shift register having an input and an output, said output of said shift register providing said output of said shift element; and

a shift mux having a data input coupled to the output of the storage element of said first matrix entry, a data input coupled to the output of the shift element of the preceding matrix entry in the same column, and a control input coupled to said set of control lines, and an output coupled to the input of said shift register.

13. The cross-connect of claim 9, wherein:

for each of said plurality of matrices, said last matrix entry of each of the columns of the matrix collectively provide an output of said matrix; and

the output of each of said plurality of matrixes is coupled to a different one of said line cards.

14. The cross-connect of claim 9, wherein:

for each of said plurality of matrices, the set of control lines for each row of the matrix control said store muxes and storage elements to selectively store in any given row on a row-by-row basis data from any one of said different line card.

15. The cross-connect of claim 9, wherein:

for each of said plurality of matrices, the set of control lines for each row of the matrix control said shift elements to move data on a row-by-row basis in said matrix.

16. A cross-connect comprising:

a plurality of sets of data input lines, each of said sets of data input lines to be coupled to a different line card;

a plurality of matrix means, each matrix means coupled to all of said sets of data input lines to selectively store, reorder, and intermix data from said different line cards, each matrix means having a output coupled to a different one of said lines cards.

17. A method comprising:

providing on given intervals to each of a plurality of matrices a plurality of ordered bits from every one of a plurality of different line cards;

for each of said plurality of matrices,

selectively storing on given intervals in any given row of the matrix the plurality of ordered bits from one of said plurality of different line cards, wherein said rows are coupled in series, and

selectively moving on given intervals data in one row of the matrix to a next row in the series; and

providing on given intervals to each of said plurality of different line cards the plurality of ordered bits from the last row of a different one said plurality of matrices.

18. The method of claim 17, wherein:

the bits in the same bit positions according to said order from each of said plurality of different line cards are groups into bit position groups; and

said selectively storing includes:

providing a different one of said bit position groups to each column of the matrix, wherein the same bit position group is provided to every matrix entry in that column.

19. The method of claim 17, wherein said selectively storing and said selectively moving further comprises:

providing a different set of control signals to each row of the matrix, wherein the set of control signals is provided to every matrix entry in that row.